REMARKS

Claims 1-25 are currently pending in this patent application. Claims 1-25 are again rejected under 35 U.S.C. 102(e) as being anticipated by Pehlke et al. (US 2005/0032488 A1), and the rejection has been made final. This rejection is respectfully disagreed with, and is traversed below.

The arguments advanced in the previous response are herewith repeated and incorporated by reference herein in their entirety.

In section 4 of the most recent office action ("Response to Arguments") the Examiner has taken issue with the arguments advanced in the previous response.

The Examiner states that the previous argument was drawn to features "not recited in the rejected claims", most specifically in the context of the previous distinction made between the VREF disclosed in the instant patent application and the VREF signal of Pehlke et al.

It is pointed out that the previous argument with regard to VREF was made to point out a distinction that is clearly recited in the independent claims. That is, and to referring an element of each of the independent claims 1, 9, 17 and 21, as in claim 1:

> "compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, **and the current output power level of the power amplifier module**." (emphasis added)

It was stated that there is no similar teaching in Pehlke et al., and no suggestion of the claimed subject matter. This fact alone should be sufficient to traverse the rejection applied under 35 U.S.C. 102(e).

Independent claim 17 claims in part a RF power amplifier module that further comprises circuitry for automatically compensating the output transistor for impedance variations appearing at the

output node due at least in part to a change in an RF propagation environment of the antenna, the circuitry comprising detection circuitry for generating a first detection signal having a value that is indicative of the current flowing through the output transistor and a second detection signal having a value that is indicative the voltage appearing at the output of the output transistor, and **further comprising compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, respectively, and the value of a signal that is indicative of a current output power level of the RF power amplifier module**, further comprising an impedance matching circuit coupled between the output of the output transistor and the output node, the impedance matching circuit presenting a variable impedance that is controlled by an output signal from the compensation circuitry, where the output signal from the compensation circuitry is generated to have a value that is a function of the value of the first detection signal and the value of the signal that is indicative of the current output power level of the RF power amplifier module.

Independent claim 20 recites in part that a RF power amplifier is contained within a package and is operable:

> "**over a range of output power levels specified by a value of a power control signal** that is one of applied to a first input of the package and generated internally to the package, the RF power amplifier comprising at least one output transistor having an input coupled to second input of the package for receiving an input RF signal and an output coupled to an output of the package for outputting an amplified RF signal, the RF power amplifier further comprising circuitry integrated with the at least one output transistor for automatically compensating the RF amplifier for impedance variations appearing at the first output, the circuitry comprising detection circuitry for generating detection signals indicative of current flowing through the at least one output transistor and of a voltage appearing at the output of the at least one output transistor, and further comprising load line compensation circuitry responsive to the detection signals **and to the power control signal** for maintaining a desired output linearity of the amplified RF signal."

The reference was then made to page 9, lines 10-13, of the instant specification:

> "In addition, the power detector 30, 32 outputs are matched to the internal (or external) reference voltage Vref. **The value of Vref is proportional to the desired output power from the PA**. That is, during normal operation the value of Vref varies up and down, depending on the PA output power" (emphasis added).

It was then stated that while Pehlke et al. do make a reference to VREF, they make it in the following (different) context (see, for example, paragraph 0078):

> "The voltage drop across the reference regulating transistor 40A, e.g., the drain-to-source drop if 40A is a FET, is sensed and amplified by a factor A_{VREF} by amplifier 60, and compared against the corresponding voltage drop across the PA's regulating transistor 40B, which is sensed and amplified similarly by a factor A_{VPA} by amplifier 62. These sensed and amplified voltages, which represent the relative instantaneous headroom to the supply voltage upper rail of each branch, are then compared in amplifier 64 and used to lock the loop by driving the gate of transistor 40B, which regulates current into PA 12.

Reference can also be made to paragraph 0080.

It was stated that clearly the VREF of Pehlke et al. is not equivalent to the Vref or VREF disclosed in the instant patent application.

However, and as should be clear when the argument is read in its entirety and in context, the reference to VREF by the Applicants was made to point out and emphasize that the claimed subject matter: "compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, **and the current output power level of the power amplifier module**" (emphasis added) was not disclosed by Pehlke et al., since VREF is disclosed in the instant patent application as being the signal that is indicative of the "current output power level of the power amplifier module", and no similar signal is seen to be used by Pehlke et al.

The Examiner then states in the Response to Arguments section, in response to the foregoing,

that Pehlke et al. teach in paragraph [0068] that the "detection circuit 48 can be configured to generate a detection signal in proportion to the detected voltage difference(s), and the control circuit 50 can be configured to generate a compensation signal responsive thereto". The Examiner then quotes paragraph [0042], followed by paragraph [0073].

Paragraph [0042] discusses the operation of the current source 14 (Figure 4) in response to the voltage-mode amplitude information signal AM_{IN} in supplying the power amplifier supply current I_{PA}. As is stated:

"[0042] In operation, the AM_{IN} signal is generated as, or converted to, a voltage-mode signal applied to the non-inverting input of the control amplifier 16, which may, for example, be an operational amplifier. The control amplifier 16 generates a control voltage based on the difference between the AM_{IN} signal and a feedback signal taken from the supply current path of the power amplifier 12. The control voltage sets the gate bias for the pass transistor 16, which in turn sets the magnitude of the supply current I_{PA} provided to the power amplifier 12."

Paragraph [0073] states:

"[0073] As another alternative, FIG. 12 depicts a control arrangement wherein circuit 46 generates a compensation signal that is used to change the bias of a power amplifier 56 responsive to detecting changes in the effective DC resistance of the power amplifier 56. It also should be understood that power amplifier 56 may be the same as the previously illustrated power amplifier 12, and that a different reference number is used primarily to highlight the bias control input."

These two paragraphs, and the associated Figures 4 and 12, have been carefully reviewed, and it is not seen where there is a disclosure of all of the elements of at least the independent claims, at least as they pertain to: "**compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals** to have values that are a function of the values of the first and second detection signals, **and the current output power level of the**

power amplifier module" (emphasis added).

If the Examiner believes that the AM_{IN} signal meets the claim limitation he is respectfully disagreed with, as the AM_{IN} signal is clearly disclosed to simply be the signal that controls the magnitude of the supply current provided to the PA 12.

This being the case, Pehlke et al. clearly do not teach the claimed subject matter. That is, the previous reference to VREF by the Applicants was made in the context of a feature that is clearly recited in the independent claims, which is a feature not disclosed by Pehlke et al. Thus, the rejection of the independent claims as being anticipated by Pehlke et al., for at least this one reason alone, is not appropriate and should be withdrawn.

If the Examiner believes otherwise, i.e., that Pehlke et al. do disclose the claimed subject matter of "compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, **and the current output power level of the power amplifier module**" (emphasis added), then he is respectfully requested to point out with more specificity where this element of the independent claims is disclosed by Pehlke et al. Absent such a showing, the final rejection of the claims as being anticipated by Pehlke et al. should be withdrawn.

It is also again pointed out that this patent application claims (e.g., as in claim 1), "compensation circuitry for controlling the **generation of a plurality of power amplifier bias current and bias voltage signals**". This subject matter as well is not seen to be expressly disclosed or suggested by Pehlke et al., such as in paragraphs 0066, 0079 and 0080, as stated by the Examiner.

In that all of the independent claims are allowable over Pehlke et al., all of the dependent claims are allowable as well for at least this one reason alone.

Note, for example, the claim 3 recites a power amplifier module as in claim 2, "where the output signal from the compensation circuitry is generated to have a value that is a function of the value

It is also again pointed out that this patent application claims (e.g., as in claim 1), "compensation circuitry for controlling the **generation of a plurality of power amplifier bias current and bias voltage signals**". This subject matter as well is not seen to be expressly disclosed or suggested by Pehlke et al., such as in paragraphs 0066, 0079 and 0080, as stated by the Examiner.

In that all of the independent claims are allowable over Pehlke et al., all of the dependent claims are allowable as well for at least this one reason alone.

Note, for example, the claim 3 recites a power amplifier module as in claim 2, "where the output signal from the compensation circuitry is generated to have a value that is a function of the value of the **first detection signal and the current output power level**" (emphasis added). However, since it has been shown that Pehlke et al. do not teach compensation circuitry that is responsive to the "current output power level", then their disclosed circuitry clearly cannot anticipate the subject matter of at least claim 3 (and 11, independent claim 17, etc.).

The Examiner is respectfully requested to reconsider and remove the rejections of the claims under 35 U.S.C. 102(e) based on Pehlke et al., and to allow all of the pending claims 1-25 as originally filed. An early notification of the allowability of claims 1-25 is earnestly solicited.

Respectfully submitted:

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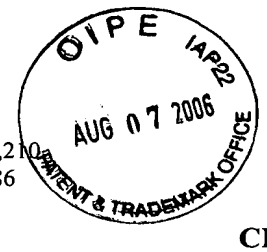

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